

ABSTRACT

5 This invention provides two circuit embodiments for a whole chip electrostatic discharge, ESD, protection scheme. It also includes a method for whole chip ESD protection. This invention relates to distributing the circuit of this invention next to each input / output pad in order to provide parallel ESD current discharge paths. The advantage of this invention is the ability to create a parallel discharge
10 path to ground in order to discharge the damaging ESD current quickly so as to avoid circuit damage. The two circuit embodiments show how the protection circuits of this invention at both the unzapped I/O pads and the zapped I/O pad are connected in a parallel circuit for discharging ESD currents quickly. These protection embodiments require a small amount of semiconductor area, since the
15 smaller protection circuits are distributed and placed at the locations of each I/O pad.